



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: FURUHATA)
Serial No.: 09/459,305)
Filed: December 10, 1999)
For: SEMICONDUCTOR DEVICES, METHODS OF)
MANUFACTURING SEMICONDUCTOR)
DEVICES, CIRCUIT SUBSTRATES AND)
ELECTRONIC DEVICES)

Group Art Unit: 2811

Examiner: Tran, T.

0015,0010

Electron
#5
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B. M. M.

RESPONSE TO ELECTION/RESTRICTION REQUIREMENT

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sirs:

In response to the Restriction Requirement dated March 7, 2001, the response being due by April 7, 2001, please enter and consider the following.

Applicant hereby elects to prosecute Group I, claims 13-19 and 26-29, drawn to a semiconductor device.

Applicant has filed together with this Response a Preliminary Amendment. Examination on the merits is respectfully requested.

Respectfully submitted,

Alan S. Raynes
Alan S. Raynes
Reg. No. 39,809
KONRAD RAYNES & VICTOR LLP
315 South Beverly Drive, Suite 210
Beverly Hills, CA 90212

Dated: April 6, 2001

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on April 6, 2001.

Alan S. Raynes
Alan S. Raynes

April 6, 2001
Date



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Assistant Commissioner for Patents
Washington, DC 20231

Dear Sirs:

Attached hereto is a Response to Election/Restriction Requirement and a Preliminary Amendment for the above-identified application. It is believed that no fee is due. Please charge any fees necessary for consideration of these papers to Deposit Account 50-0585.

Respectfully submitted,

Alan S. Raynes

Dated: April 6, 2001

Reg. No. 39,809

KONRAD RAYNES & VICTOR LLP
315 South Beverly Drive, Suite 210
Beverly Hills, CA 90212

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Alan S. Raynes
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PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sirs:

Please enter and consider the following amendments and remarks.

IN THE CLAIMS:

Please amend claims 17, 26 and 29 as follows:

17. (Amended) The semiconductor device according to claim 13, wherein at least one part of the connecting area has almost the same impurity depth and almost the same impurity concentration of one of a source/drain area and an off-set area of MOS transistor forming a surrounding circuit of the first and second memory cell areas.

26. (Amended) A semiconductor device comprising:
first and second field effect transistors, each having source/drain regions; and
a conducting region connecting a source/drain of the first field effect transistor to a source/drain of the second field effect transistor, the conducting region having a lower resistance than at least one of the source/drain regions.